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DEVELOPMENT OF  $Y_2O_3$ /GRAPHENE/COPPER HETEROSTRUCTURE AS A  
SUBSTRATE MATERIAL FOR GaN EPILAYERS

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**Abstract**

In present work, graphene and  $Y_2O_3$  thin layers deposited by CVD and PLD on large size Cu foil. The AlN was grown by RF-sputtering technique at  $450^\circ\text{C}$ . The SEM and XRD analysis of AlN/ $Y_2O_3$ /graphene/Cu sample shows a smooth surface and indicate small AlN (0001) peak.

Because of the excellent optical and electrical characteristics of nitride semiconductors [1,2], full-color-spectrum nitride light-emitting diodes (LEDs) with high efficiency and reliability and long-term stability are now commercially available [3]. These results were outstanding considering the fact that the material was showing very high crystal defect densities ( $\sim 10^{19}$ - $10^{10}$  dislocations/cm<sup>2</sup>), more than 4 orders of magnitude higher than those in III-As or III-P LEDs [4]. The defects seen in nitride LEDs mainly result from stresses due to their epitaxial growth on foreign substrates. These substrates exhibit differences in lattice parameter, chemical composition and coefficient of thermal expansion (CTE) with GaN. LED manufacturing processes require continuous improvement of the layer quality, wafer uniformity and reproducibility of the epitaxial growth process in order to reduce the production cost and increase wafer size. SiC has lattice and thermal mismatches of 4% and 25% respectively with GaN, and good thermal conductivity. However, SiC has high defect density, including severe influence on epi-GaN quality by SiC micro-pipe dislocation defects.

The present work is devoted to deposition of graphene as an intermediate layer between the GaN layer and a metal substrate. Graphene films exhibit high temperature stability, optical transparency, mechanical flexibility, and high electrical and thermal conductivity. Graphene films can now be grown on a large scale on metal foils of Cu, Ni and their alloys. We believe that our approach at using graphene intermediate layers on a metal substrate has two specific advantages: First, the honeycomb lattice structure of the graphene template can offer a platform and flexibility for selected buffer material with hexagonally symmetric lattice structure and (0001) orientation, which may well match that of AlN and GaN. Second, due to the self-assembling and surface inert properties of graphene, the transfer of the material and devices fabricated on graphene onto other substrates will be quite direct.

Such an approach would yield two layers with a 6.1% lattice mismatch (SiC and graphene) – typically too large for good epitaxial growth (lattice mismatch should be less than 2-3%). To further mitigate this lattice mismatch, a  $Y_2O_3$  buffer layer is proposed to be grown by PLD between the graphene and the SiC layer thus having a 1.55% lattice mismatch with graphene in a 1:6 unit cell ratio, and a 2.6% mismatch with SiC. The net mismatch would be less than for SiC directly on graphene. Such a Cu/graphene/ $Y_2O_3$ /SiC heterostructure exhibiting a minimization of lattice mismatch for highly epitaxial growth of SiC on graphene, would support the high temperature